DRAM MODULE

1 MEG x 8

1 MEGABYTE, 5V,
FAST PAGE MODE

FEATURES

- JEDEC- and industry-standard pinout in a 30-pin, single-in-line memory module (SIMM)
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 6mW standby; 450mW active, typical
- All device pins are TTL-compatible
- FAST PAGE MODE (FPM) access cycle
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- Low profile
- 1,024-cycle refresh distributed across 16ms

OPTIONS MARKING

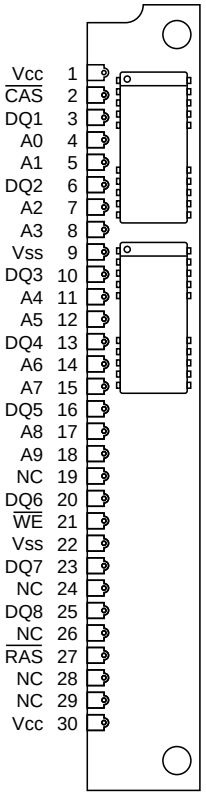
- Timing
  60ns access -6
  70ns access -7
- Packages
  30-pin SIMM M
- Part Number Example: MT2D18M-6

KEY TIMING PARAMETERS

SPEED	t_{RC}	t_{RAC}	t_{PC}	t_{AA}	t_{CAC}	t_{RP}
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

PIN ASSIGNMENT (Front View)

30-Pin SIMM
(DD-1)



GENERAL DESCRIPTION

The MT2D18 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x8 configuration. During READ or WRITE cycles, each word is uniquely addressed through 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Early WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, and the output pins remain open (High-Z) until the next $\overline{CAS}$ cycle.

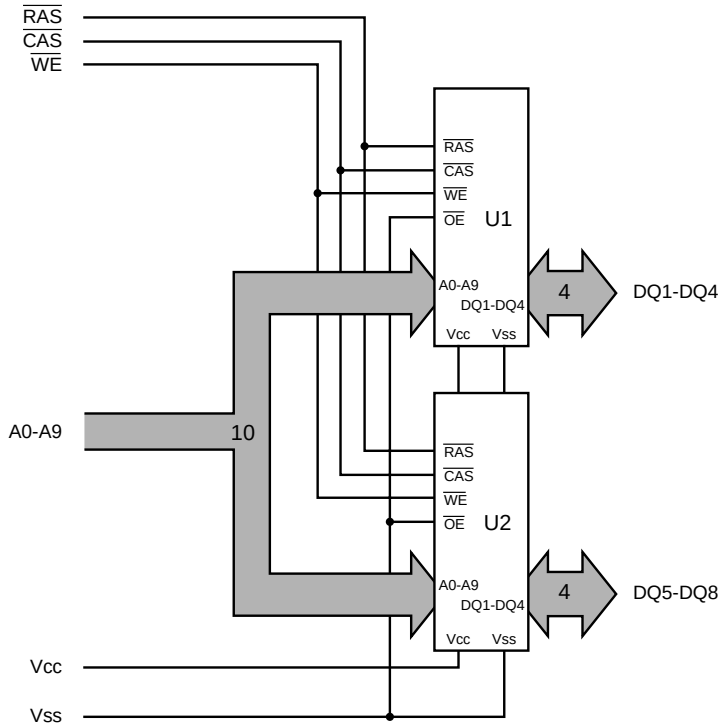
FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles.

REFRESH

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U2 = MT4C4001JDJ

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA-IN/OUT
					^tR	^tC	DQ1-DQ8
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +125°C
Power Dissipation 2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.4	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE Any input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	A0-A9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	I_I	-4	4	µA	
OUTPUT LEAKAGE (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	DQ1-DQ8	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low (Logic 0) Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

		MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	4	4	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	2	2	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	220	200	mA	2, 26, 28
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	160	140	mA	2, 26, 28
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	220	200	mA	26, 28
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	220	200	mA	19, 26

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		13	pF	17
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		17	pF	17
Input/Output Capacitance: DQ1-DQ8	C_{IO}		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		30		35	ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		ns	
Column-address setup time	^tASC	0		0		ns	
Row-address setup time	^tASR	0		0		ns	
Access time from $\overline{CAS}$	^tCAC		15		20	s	9
Column-address hold time	^tCAH	10		15		ns	
$\overline{CAS}$ pulse width	^tCAS	15	10,000	20	10,000	ns	
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		ns	
$\overline{CAS}$ precharge time	^tCP	10		10		ns	18
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		ns	
$\overline{CAS}$ hold time	^tCSH	60		70		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		ns	19
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	
Data-in hold time	^tDH	10		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Data-in setup time	^tDS	0		0		ns	15
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	12, 27
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a	21
Access time from $\overline{RAS}$	^tRAC		60		70	ns	8
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	22
Row-address hold time	^tRAH	10		10		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	
$\overline{RAS}$ pulse width	^tRAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

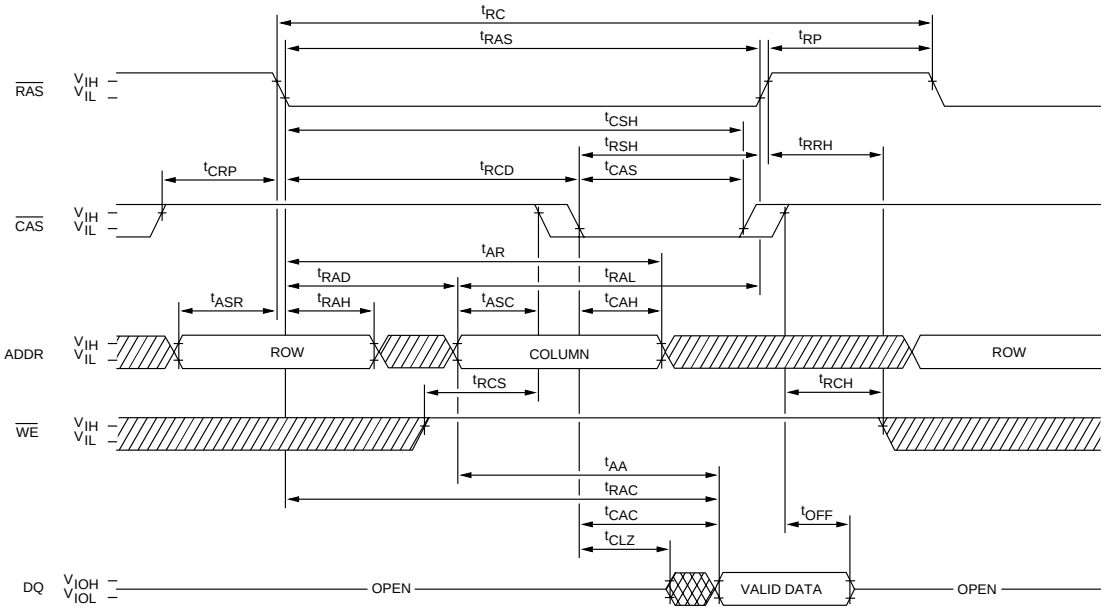
(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^{t}RC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^{t}RCD	20	45	20	50	ns	13
Read command hold time (referenced to $\overline{CAS}$)	^{t}RCH	0		0		ns	24
Read command setup time	^{t}RCS	0		0		ns	
Refresh period (1,024 cycles)	^{t}REF		16		16	ms	
$\overline{RAS}$ precharge time	^{t}RP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		ns	
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		ns	24
$\overline{RAS}$ hold time	^{t}RSH	15		20		ns	
READ WRITE cycle time	^{t}RWC	n/a		n/a		n/a	21
Write command to $\overline{RAS}$ lead time	^{t}RWL	15		20		ns	
Transition time (rise or fall)	^{t}T	3	50	3	50	ns	
Write command hold time	^{t}WCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	45		55		ns	
$\overline{WE}$ command setup time	^{t}WCS	0		0		ns	
Write command pulse width	^{t}WP	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^{t}WRH	10		10		ns	23
$\overline{WE}$ setup time (CBR REFRESH)	^{t}WRP	10		10		ns	23

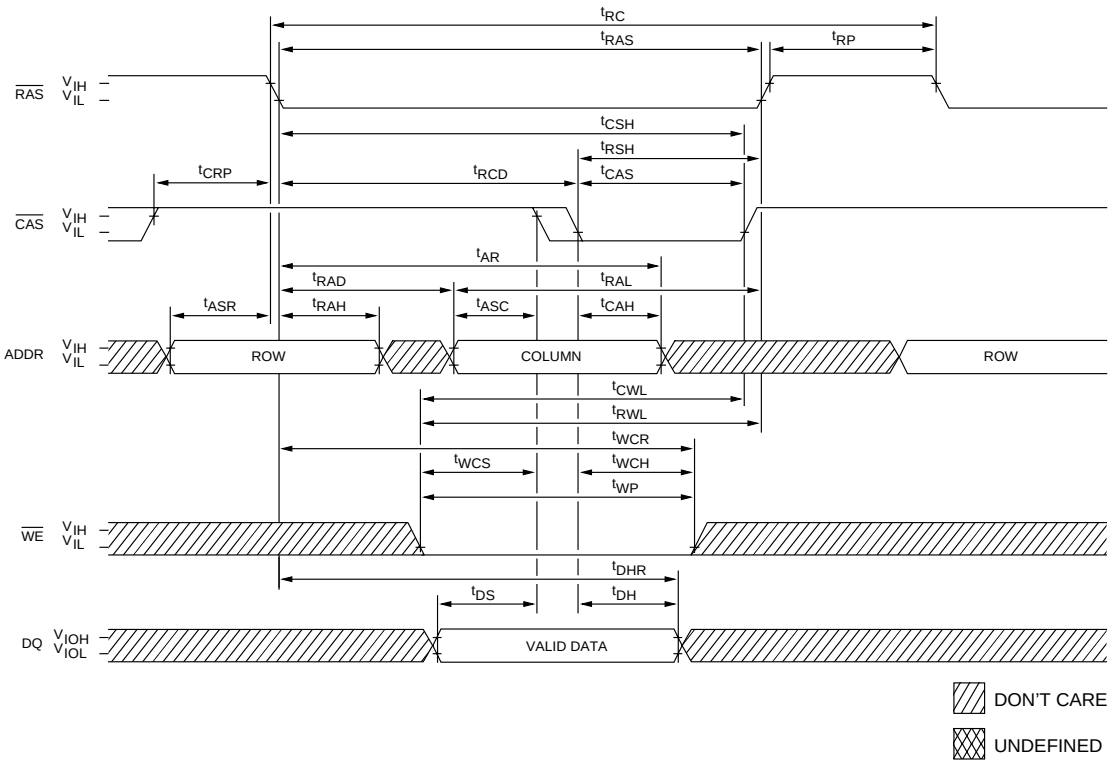
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume $^{t}T = 5ns$.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that $^{t}RCD \ge {}^{t}RCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. ^{t}RCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, V_{CC} = 5V, DC bias = 2.4V at 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1 and U2.
22. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
23. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
24. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
25. All other inputs at V_{CC} -0.2V.
26. I_{CC} is dependent on cycle rates.
27. The 3ns minimum is a parameter guaranteed by design.
28. Column-address changed once each cycle.

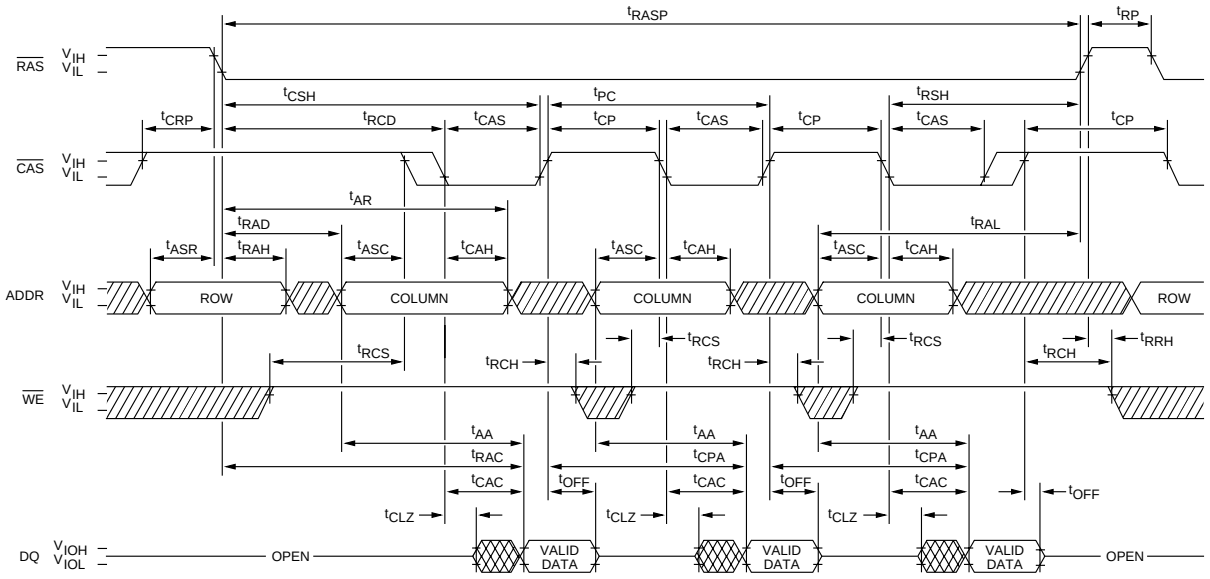
READ CYCLE



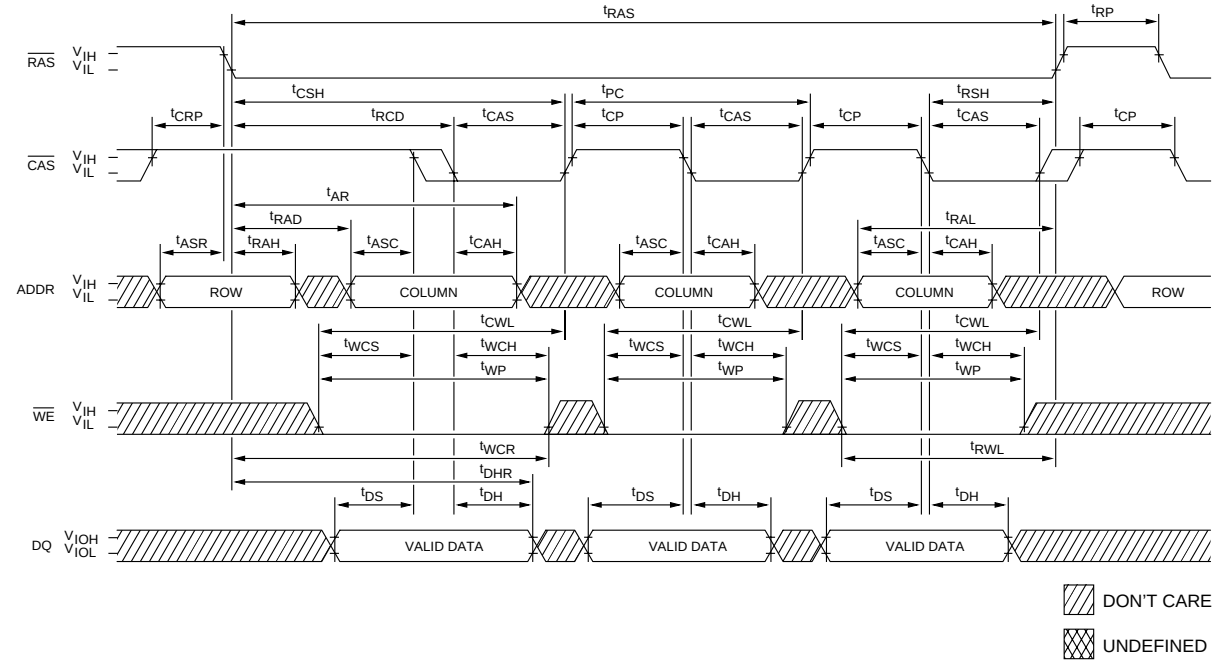
EARLY WRITE CYCLE



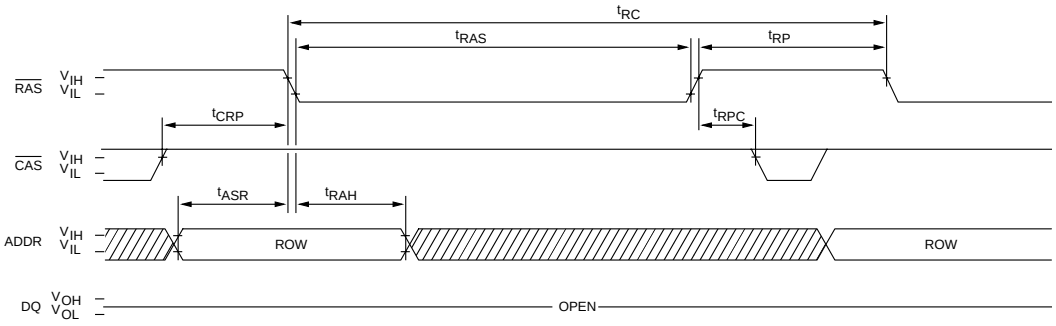
FAST-PAGE-MODE READ CYCLE



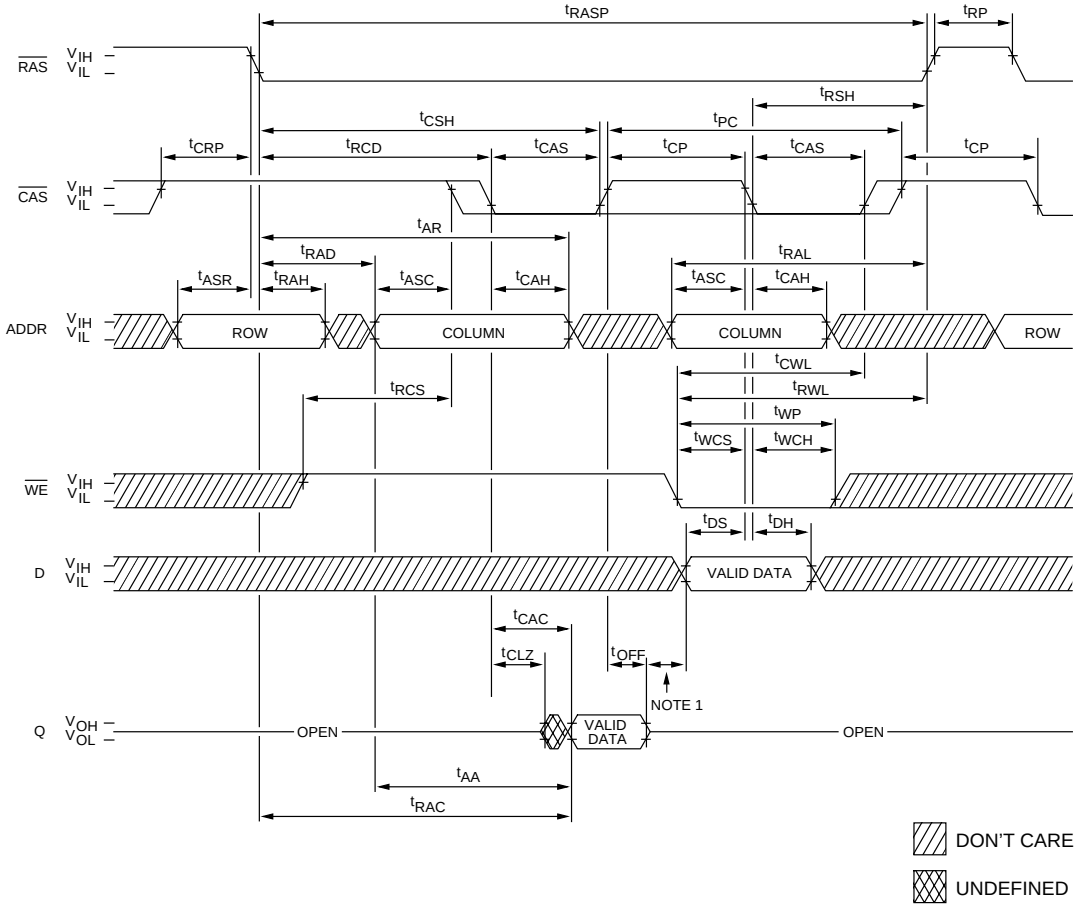
FAST-PAGE-MODE EARLY-WRITE CYCLE



$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
($\overline{\text{WE}}$ = DON'T CARE)

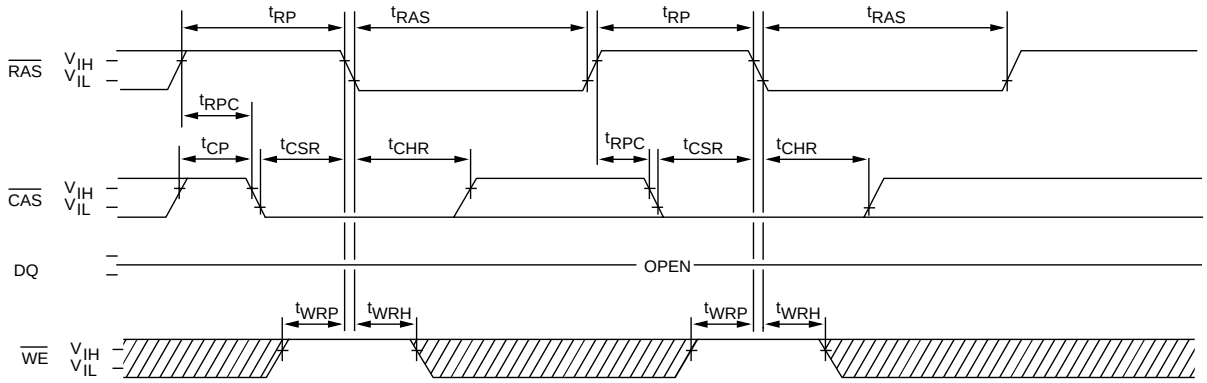


FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

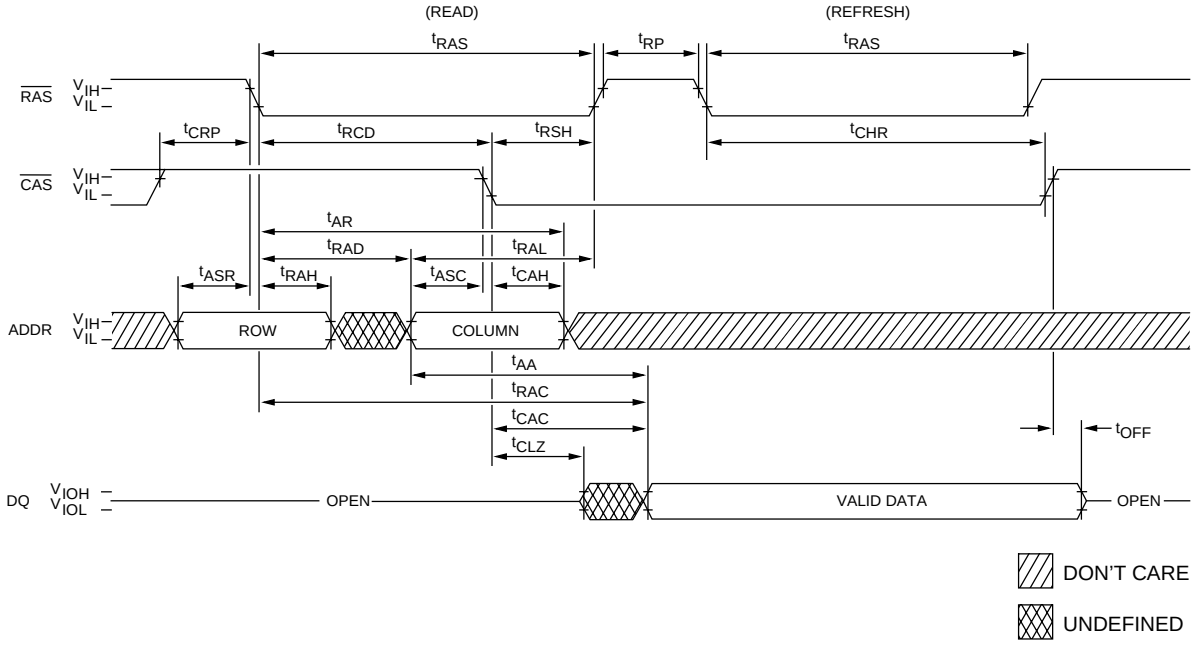


NOTE: 1. Do not drive data prior to tristate.

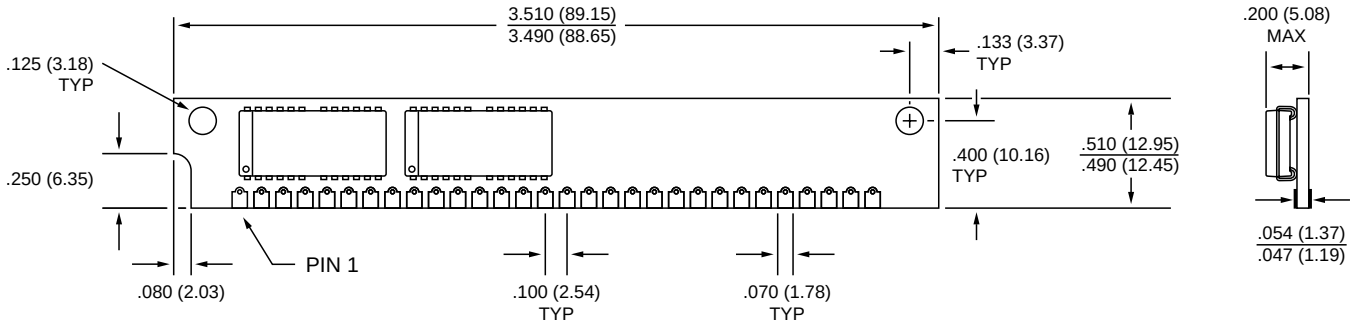
CBR REFRESH CYCLE
(Addresses = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH)



30-Pin SIMM



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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